

**REMARKS**

In the present Amendment, the specification has been amended at page 124, line 30, to add “palladium” and “the like” to the examples of the metal particles, i.e., copper, gold, silver, aluminum, nickel, titanium, chromium, tin/lead and platinum. This description is present in the specification of PCT/JP99/05003, i.e., the international stage of the present application, and which should be included but was inadvertently omitted from the translation.

Further, claim 24 has been amended to incorporate the subject matter of claim 55. Claim 32 has been amended to incorporate the subject matter of claim 57 and further recite that the thickness of each of said conductor circuit is substantially the same as the thickness of said conductor layer on said interlayer resin insulating layer. This amendment is supported by the specification, for example, at page 55, lines 4-11. Claim 37 has been amended to recite that the via holes cover the whole opening of the through holes. This amendment is supported by the specification, for example, in Figs. 36 and 37. Claim 40 has been amended to recite that the filler comprises a metal particle. This amendment is supported by the specification, for example, at page 124, lines 16-19. Claims 41 and 62 have been amended to recite that the whole surfaces of the filler are exposed from the plated-through holes. These amendments are supported by the specification, for example, in Fig. 49. Claim 42 has been amended to recite that lower-layer via holes are disposed to cover the whole opening of through holes of the plated-through holes. This amendment is supported by the specification, for example, in Fig. 50. Claims 40-42 have also been amended to delete the recitation that upper-layer via holes are disposed immediately over

said lower-layer via holes, said upper-layer via holes being interconnected with said lower-layer via holes.

Claims 64-67 have been added. Claims 64-67 are supported by the specification, for example, at page 124, lines 28-30; at page 124, lines 30-31; previously presented claims 40-42; and in Figs. 36, 46 and 50, respectively.

Claims 55 and 57 have been canceled. Claims 1-8, 14-22, 27-31, 33-36, 39 and 47 were previously canceled.

No new matter has been added and entry of the Amendment is respectfully requested. Upon entry of the Amendment, claims 9-13, 23-26, 32, 37, 38, 40-46 and 48-67 will be all the claims pending in the application.

Applicants note with appreciation that claims 9-13, 23, 25, 26, 48-53, 56 and 63 are allowed.

**I. Form PTO/SB/08 A & B**

The Examiner has not returned a signed copy of the Form PTO/SB/08 A & B filed with Applicants' Information Disclosure Statement of June 9, 2004. The Examiner is respectfully

requested to initial and date the Form and return a signed copy to Applicants' representative in the next PTO communication.

**II. Response to Rejections under 35 U.S.C. § 102**

a. At page 2 of the Office Action, claims 24, 32 and 57 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Ono (U.S. Patent 6,217, 987).

Applicants respectfully submit that the present claims are novel and patentable over Ono for at least the following reasons.

**i. Claim 24**

Ono discloses a printed circuit board, in which the conductor circuit has a roughened layer 11 which contacts the interlayer insulating resin layer 2, and has the electroless copper plated film 12 and the electrolytic copper plated film 13. The interlayer insulating resin layer 2 has a roughened surface. The lower-layer conductor circuit and the electroless plated film 12 on the bottom of the via hole are connected through the roughened surface 11 of the lower-layer conductor circuit.

However, Ono does not teach or suggest the relationship between the thickness of the electroless plated film 12 on the bottom of the via hole and the thickness of the electroless plated film 12 on the interlayer insulating resin layer 2, let alone that the electroless plated film formed

on the bottoms of the via holes has a thickness equal to 50 to 100% of the thickness of the electroless plated film on the interlayer resin insulating layer, as recited in present claim 24.

Further, the Examiner considers that Furui teaches the diameter of the via hole (related to rejection of claim 55).

However, the diameter described in Furui (col. 4, lines 30-35) is the diameter of via holes 41, which are analogous to the through hole, rather than the via hole, of the present invention.

Moreover, according to the present invention, the plating can be sufficiently conducted in the opening for the fine via hole. The diameter of the via hole is adjusted to conduct a sufficient plating (page 63, lines 2 to 7). Ono does not disclose or suggest such effects of the present invention.

ii. Claims 32 and 57

As noted above, claim 32 has been amended to incorporate the subject matter of claim 57 and claim 57 has been canceled. Claim 32 recite that the thickness of each of said conductor circuit is not greater by more than 10  $\mu\text{m}$  than the thickness of said conductor layer on said interlayer resin insulating layer. Ono does not specifically disclose this feature of the present invention.

Further, the present invention provides unexpected superiority. As described at page 55, lines 4 to 19 of the present specification, since there is not a great difference between the thickness of the conductor circuit and the thickness of the conductor layer on the interlayer resin insulating layer, an impedance alignment can be easily attained between the conductor circuit on the core board and the conductor layer on the interlayer resin insulating layer, thereby improving the high-frequency characteristic of the multilayer printed circuit board. In addition, cracks in the interlayer resin insulating layer can be prevented.

In addition, Applicants have canceled claim 57.

In view of the foregoing, Applicants respectfully submit that claims 24 and 32 are not anticipated or rendered obvious by Ono, and thus the rejection should be withdrawn.

**b.** At page 4 of the Office Action, claims 37, 40 to 46 and 62 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Chong (U.S. Patent 5, 699, 613).

Applicants respectfully submit that the present claims are novel and patentable over Chong for at least the following reasons.

Chong discloses a multiple layer circuit board structure comprising base laminate 1, conductive patterns 12 and 14 on both sides of the base laminate 1, the dielectric material 23 on

each of the conductive patterns, and the vias 24 and 26 to 29. Vias 26 and 29 are formed on the through hole 16 which extends through the base laminate 1. The through hole 16 is filled with a conductive polymer 21. The through hole 16 may be plated with a copper layer 19 before being filled with the conductive polymer 21 (Fig. 3B).

i. Claims 37, 41, 42, 62 and 67

According to the present invention (claims 37 and 42), the via holes formed immediately over the plated-through holes cover the whole opening of the through holes in the plated-through holes. Further, the plated film of the lower-layer via hole connects with the plated film of the plated-through hole (claim 67). Connection of the via hole and the plated-through hole is thereby ensured.

However, Chong does not teach or suggest that the whole opening of the through hole 16 is covered with the vias 26 and 29. Further, Chong teaches that the plating 31 constituting the vias contacts with the conductive polymer 21 (metal-polymer contact).

According to the present invention (claim 67), on the other hand, the plated film constituting the via hole is connected with the plated film constituting the plated-through hole (metal-metal contact). Since the metal-metal contact has a relatively low contact resistance, it is advantageous to increase the signal transmission speed. In addition, a firm contact is realized and connection reliability improves.

Furthermore, according to the present invention (claims 41 and 62), the whole surface of the filler exposed from the plated-through hole is covered with the conductor layer.

However, Chong does not teach or suggest that the whole surface of the conductive polymer 21 is covered with a conductor layer.

In view of the above, Chong does not teach or suggest the constitution of present independent claims 37, 41, 42 and 62, and claim 67 depending therefrom. The present invention is neither anticipated by nor obvious over Chong.

ii. Claims 40, 64 and 65

According to the present invention, the filler in the plated-through holes may comprise metal particles (claim 40) such as copper or aluminum (claim 64). In contrast, in Chong, the through hole 16 is filled with a conductive polymer 21. For this reason, the constitution of the present invention is different from that of Chong.

Further, the metal particles increase the conductivity through the plated through hole. Further, the metal particles exposed from the surface of the filler are integrated with the conductor layer formed thereon, and the exfoliation of the conductor layer is thereby prevented (page 124, lines 16 to 25 of the present specification). Metal such as copper or aluminum does

not influence the electric property of the filler since it has a relatively low resistivity. Diameter of the metal particles is preferably within the range of 0.1 to 50  $\mu\text{m}$  to maintain a good wettability against the resin and a high printing efficiency.

iii. Claim 44

Chong teaches that the vias are filled with conductive polymer 32 (col. 4, lines 57 to 61). According to the present invention, on the other hand, the lower-layer via hole may be filled with metal (claim 44). Accordingly, the constitution of the present invention is different from that of Chong.

iv. Claim 66

In the present invention, the upper-layer via holes are disposed immediately over the lower-layer via holes and interconnected with the lower-layer via holes. The wiring length can thereby be decreased to increase the signal transmission speed.

In view of the foregoing reasons, Applicants respectfully submit that the present claims are not anticipated or rendered obvious by Chong, and thus the rejections based on Chong should be withdrawn.



**III. Response to Rejections under 35 U.S.C. § 103**

a. At page 7 of the Office Action, claim 54 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Ono in view of Greschner (U.S. Patent 4,642,163).

Applicants respectfully submit that claim 54 is patentable over Ono in view of Greschner for at least the following reasons.

Greschner teaches a method for forming an electroless copper layer 7 on a sputtered copper layer 6. The Examiner considers that Greschner teaches an electroless plating solution containing tartaric acid.

Applicants disagree. Specifically, the plating solution described at col. 6, lines 15 to 20 of Greschner, contains  $\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$ ,  $\text{HCHO}$ ,  $\text{NaCN}$  and AEDTA and not tartaric acid. In particular, EDTA is ethylenediaminetetraacetic acid, i.e.

$(\text{HOOCCH}_2)_2\text{NCH}_2\text{CH}_2\text{N}(\text{CH}_2\text{COOH})_2$ , which is different from tartaric acid of the formula  $(\text{HOOC})\text{CH}(\text{OH})\text{CH}(\text{OH})(\text{COOH})$ .

Further, the present invention, which is directed to a plating solution containing tartaric acid, provides a plated layer which adheres intimately to the substrate and hardly peels off (page 34, lines 19 to 26 of the present specification). Greschner does not teach or suggest use of such a plating solution containing tartaric acid, let alone the effects thereof.

Accordingly, even if, *arguendo*, there might be motivation to combine the cited references, the combination still would not result in the present invention.

In view of the foregoing, Applicants respectfully submit that claim 54 is not obvious over Ono in view of Greschner, and thus the rejection should be withdrawn.

**b.** At page 9 of the Office Action, claim 38 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Chong in view of Furui (U.S. Patent 5,258,094).

Applicants respectfully submit that claim 38 is patentable over Chong in view of Furui for the same reasons as set forth in Section II.b (see page 17 et seq.) and the following additional reasons.

Furui discloses a multilayer printed wiring board comprising a through hole 41. Furui teaches that the multilayer printed wiring board comprises the photoviahole 42 connecting the 2nd conductive layer 62 and the 3rd conductive layer 63. However, the photoviahole is not formed on the through hole 41, and does not cover the through hole 41. Therefore, Furui does not rectify the deficiencies of Chong.

Moreover, according to the present invention, when the diameter of the through holes in said plated-through holes is 200  $\mu$ m or less, the size of the via holes covering the whole opening of the through holes is not too large, and the wiring density is not decreased (page 69, lines 29 to 34 of the present specification). Further, the contact between the through hole and the via hole is ensured to decrease the contact resistance.

On the other hand, Chong does not teach that the vias cover the whole opening of the through hole 16. Accordingly, it is not necessary to adjust the diameter of the through hole 16.

In view of the foregoing, Applicants respectfully submit that even if, *arguendo*, there might be motivation to combine Chong and Furui, the combination still would not result in the present invention. Further, there is no motivation to adjust the diameter of the through hole of Chong so that the whole opening of the through hole is covered by a small-sized via hole. Therefore, the Examiner is respectfully requested to reconsider and withdraw the rejection.

c. At page 9 of the Office Action, claim 55 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Ono in view of Furui.

Applicants respectfully submit that the rejection is moot because claim 55 has been canceled.

d. At page 10 of the Office Action, claims 58 and 60 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Chong in view of Watada (U.S. Patent 6,225,396).

Applicants respectfully submit that claims 58 and 60 are patentable over Chong in view of Watada for the same reasons as set forth in Section II.b (see page 17 et seq.) and the following addition reasons.

Watada discloses a resin composite and that an epoxy resin containing silica particles can be used as a material for a resin composite. Watada does not rectify the deficiencies of Chong.

Therefore, even if, *arguendo*, there might be motivation to combine the cited references, the combination still would not result in the present invention. Accordingly, Applicants respectfully submit that claims 58 and 60 are not obvious over Chong in view of Watada, and thus the rejection should be withdrawn.

e. At page 11 of the Office Action, claims 59 and 61 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Chong in view of Ono.

Applicants respectfully submit that claims 59 and 61 are patentable over Chong in view of Ono for the same reasons as set forth in Section II.b (see page 17 et seq.). In addition, Ono does not rectify the deficiencies of Chong. Therefore, even if, *arguendo*, there might be

motivation to combine the cited references, the combination still would not result in the present invention. Accordingly, Applicants respectfully submit that claims 59 and 61 are not obvious over Chong in view of Ono, and thus the rejection should be withdrawn.

**IV. Conclusion**

In view of the above, reconsideration and allowance of claims 9-13, 23-26, 32, 37, 38, 40-46 and 48-67 are now believed to be in order, and such actions are hereby earnestly solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the local Washington D.C. telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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